CLAIMS

What is claimed is:

1. A method for implementing a programmable chip, the method comprising:

receiving input information identifying a desired module and a desired input data rate associated with the desired module, wherein the input information is received at a design tool used to implement a programmable chip;

identifying a plurality of candidate modules, the plurality of candidate modules having simulation information indicating associated data rates; and

selecting an optimal candidate module from the pool of candidate modules, the optimal candidate module selected using the desired input data rate.

2. The method of claim 1, further comprising receiving a desired output latency associated with the desired module

3. The method of claim 2, wherein the optimal candidate module is selected using the desired input data rate and the desired output latency.

4. The method of claim 2, wherein simulation information also indicates output latencies.

5. The method of claim 4, wherein receiving the desired data rate and the desired output latency allows selection of the optimal candidate module without having to receive information on clock frequency.

6. The method of claim 1, further comprising using time-domain multiplexing if the optimal candidate module runs at a data rate substantially faster than the desired input data rate.

7. The method of claim 6, further comprising generating a clock synthesis circuit to allow multiplexing.

8. The method of claim 7, wherein the clock synthesis circuit comprises a phase lock loop.

9. The method of claim 7, wherein the clock synthesis circuit comprises a delay lock loop.

10. The method of claim 1, further comprising using multiple instantiations of the optimal candidate module if the optimal candidate module runs at a data rate substantially slower than the desired input data rate.

11. The method of claim 1, wherein the plurality of candidate modules are associated with chip area usage requirements and power requirements.

12. The method of claim 11, wherein chip area usage requirements and power requirements are used as factors in selecting the optimal candidate module.

13. The method of claim 1, further comprising performing timing simulation using the optimal candidate module.

14. The method of claim 1, further comprising receiving system clock information.

15. A computer program product comprising a machine readable medium on which is provided program instructions for implementing a programmable chip, the program instructions comprising:

instructions for receiving input information identifying a desired module and a desired input data rate associated with the desired module, wherein the input information is received at a design tool used to implement a programmable chip;

instructions for identifying a plurality of candidate modules, the plurality of candidate modules having simulation information indicating associated data rates; and

instructions for selecting an optimal candidate module from the pool of candidate modules, the optimal candidate module selected using the desired input data rate.

16. The computer program product of claim 15, further comprising instructions for receiving a desired output latency associated with the desired module

17. The computer program product of claim 16, wherein the optimal candidate module is selected using the desired input data rate and the desired output latency.

18. The computer program product of claim 16, wherein simulation information also indicates output latencies.

19. The computer program product of claim 18, wherein instructions for receiving the desired data rate and the desired output latency allows selection of the optimal candidate module without having to receive information on clock frequency.

20. The computer program product of claim 15, further comprising instructions for using time-domain multiplexing if the optimal candidate module runs at a data rate substantially faster than the desired input data rate.

21. The computer program product of claim 20, further comprising instructions for generating a clock synthesis circuit to allow multiplexing.

22. The computer program product of claim 21, wherein the clock synthesis circuit comprises a phase lock loop.

23. The computer program product of claim 21, wherein the clock synthesis circuit comprises a delay lock loop.

24. The computer program product of claim 15, further comprising instructions for using multiple instantiations of the optimal candidate module if the optimal candidate module runs at a data rate substantially slower than the desired input data rate.

25. The computer program product of claim 15, wherein the plurality of candidate modules are associated with chip area usage requirements and power requirements.

26. The computer program product of claim 25, wherein chip area usage requirements and power requirements are used as factors in selecting the optimal candidate module.

27. The computer program product of claim 15, further comprising instructions for performing timing simulation using the optimal candidate module.

28. The computer program product of claim 15, further comprising instructions for receiving system clock information.

29. An apparatus for implementing a programmable chip, the apparatus comprising:

a design tool used to implement a programmable chip and configured to

receive input information identifying a desired module and a desired input data rate associated with the desired module;

identify a plurality of candidate modules, the plurality of candidate modules having simulation information indicating associated data rates; and

select an optimal candidate module from the pool of candidate modules, the optimal candidate module selected using the desired input data rate.

30. The apparatus of claim 29, further comprising having the design tool configured to receive a desired output latency associated with the desired module

31. The apparatus of claim 30, wherein the optimal candidate module is selected using the desired input data rate and the desired output latency.

32. The apparatus of claim 30, wherein receiving the desired data rate and the desired output latency allows selection of the optimal candidate module without having to receive information on clock frequency.

33. The apparatus of claim 29, further comprising having the design tool configured to use time-domain multiplexing if the optimal candidate module runs at a data rate substantially faster than the desired input data rate.

34. The apparatus of claim 33, further comprising having the design tool configured to generate a clock synthesis circuit to allow multiplexing.

35. The method of claim 29, further comprising having the design tool configured to use multiple instantiations of the optimal candidate module if the optimal candidate module runs at a data rate substantially slower than the desired input data rate.

36. The method of claim 29, wherein the plurality of candidate modules are associated with chip area usage requirements and power requirements that are used as factors in selecting the optimal candidate module.

37. The method of claim 29, further comprising having the design tool configured to perform timing simulation using the optimal candidate module.

38. The method of claim 29, further comprising having the design tool configured to receive system clock information.